Implementation of Sequential Circuits using Quantum dot cellular automata.

Aparajit Shrivastava*,

* Shriram College of Engineering and Technology
Department of Computer Science and Engineering, RGPV University, Gwalior, India

Abstract—This challenging and interesting problem has attract researcher/scientist for various background i.e. psychology, electronics, artificial intelligence, parallel computing, soft computing, quantum computing and nano computing. This paper involves the study and implementation of Quantum dot cellular automata, referred to hereafter as QCA. QCA provides for nanolevel computations using molecular components as computational units. In this paper, RS & JK flip-flops are designed and analyzed using the software QCA Designer. Quantum Dot Cellular Automata has attractive features such as faster speed, smaller size and low power consumption than transients-based technology. The proposed structures of RS & JK flip-flops are simulated using QCA Designer. Thus it is interesting to think of the consequences this new technology could have for many logic circuits and digital systems. It is also useful to consider how existing logic could be realized using the new technology.

Keywords: QCA, Quantum Dot, Nano computing, Cellular Automata, QCA Designer, Logic gates, RS and JK Flip-Flops.

I. INTRODUCTION

Quantum-Dot Cellular Automata (QCA) is an emerging paradigm which allows operating frequencies in range of THz and device integration densities about 900 times more than the current end of CMOS scaling limits, which is not possible in current CMOS technologies. It has been predicted as one of the future nanotechnologies in Semiconductor Industries Association’s International Roadmap for Semiconductors (ITRS, [1]). QCA encodes information in the configuration of electrons within the QCA cell, and relies on charge interactions to enable the transmission and processing of information. Logical operations and data movement are accomplished via Coulombic interaction between neighboring QCA cells rather than electric current flow.

The logic unit in QCA is the QCA cell which was proposed by researchers at the University of Notre Dame. The QCA cell is composed of 4 or 5 quantum dots. Before we examine the potential functionality of these cells we need to know a few basic facts about quantum dots. A quantum dot is a nanometer sized structure that is capable of trapping electrons in three dimensions.

This paper presents flip-flop (FF) devices as well as circuits. This FF extends a previous threshold-based configuration to QCA by taking into account the timing issues associated with the adiabatic switching of this technology. Unique timing constraints in QCA sequential logic design are defined and investigated. This has been able to come up with a design for a flip-flop used in semiconductor devices. However, it is failed to extend the design to have a universal paradigm for synchronous circuit design using quantum cells. This is an area which probably requires a new way of thinking about state encoding and finite state automata to come up with a general approach. This remains our area of further query into this fascinating subject. The goal of this work is make the flip-flops which have the different design from the flip-flops build in traditional CMOS circuit. A simulation result shows the flip flop behavior as the input and output in this paper. This design seems a very mechanical task; it is in fact a very tricky and non trivial on particularly with respect to deciding the clocking zones.

II. SIMULATION ENGINES

Currently, QCA Designer has two distinct simulation engines available. Each of the two engines has a different and important set of benefits and drawbacks.

A. Digital Simulation Engine

The digital simulation engine is a binary logic simulator within QCA Designer. This engine considers each cell to be in one of three states: null, logical one, or logical zero. With these three states and the appropriate clocking zone information for each cell, a design can be quickly simulated to ensure that for a given set of inputs, the correct set of outputs will be produced desired logic function. The advantage of this simulator is that a designer can quickly see the logic functionality of a system is desired. Since no physical information outside of cell locations and orientation is needed by the simulator, it should remain an integral part of QCA Designer throughout its lifetime.

B. Two-State Simulation Engine

To facilitate more accurate simulations we require a more advanced simulation engine [02]. The two-state model assumes that the cell is a simple two state system, for which the Hamiltonian is given by

$$H = \sum_j \begin{pmatrix} -P, & \frac{1}{2} E^{k_j}, & -\gamma_j \ 
\ -\gamma_j, \ & P, \ & \frac{1}{2} E^{k_j}, \ 
\ -P, & \gamma_j, \ & P \end{pmatrix}$$

Using the Jacobi algorithm we are able to find the Eigen values and vectors of the Hamiltonian. Where Hi is the Hamiltonian given in [03], ψi is the state vector of the cell. EI is the energy associated with the state ψi. The algorithm sorts each of the states, ψi, according to their respective energy, in ascending order. The first state in the sorted list is that which has the lowest energy.
Our assumption is that the system remains very close to the ground state during computation. As a result, the state with the lowest energy is chosen and the cell polarization is set accordingly. The two state simulation engine computes the polarization of each cell in the design until the entire system has converged to a preset tolerance. Once the system has converged, the output values are recorded, new input values are set and the simulation is reiterated. This method is less efficient in comparison to the nonlinear approximation, and as a result leads to longer simulation times. The advantage of this method is that the model on which it is based is far more accurate.

The dynamics of the QCA cell can be modeled by the many particle Schrödinger equation [04]. This exact approach is computationally intensive and becomes prohibitive when very few cells are involved. It has been shown that it is possible to model larger QCA circuits using Hartee-Fock approximation. This approach models the intracellular dynamics quantum mechanically and intercellular interactions classically by assuming that there interaction sure not coherent and purely Columbic. This approach can sometimes lead to erroneous results. This can be detected.

\[ H \psi_i = E_i \psi_i \]

In order to facilitate rapid design QCA Designer includes two important QCA models. The first uses an approximation of the cell to cell response function given by

\[ P_i = \frac{E_{k i, j}^k \sum_j P_j}{\sqrt{1 + \left( \frac{E_{k i, j}^k \sum_j P_j}{2\gamma} \right)^2}} \]

In this eq. \( P_i \) is the polarization of the cell, \( P_j \) is the polarization of other local cells \( E_{k i, j} \) is called the kink energy between cells \( i \) and \( j \), and represents the energy cost of opposite polarization in two cells. \( \gamma \) is the tunneling energy between two dots in the cell and potentially can be used to clock the cell. The ground state of the system is iteratively calculated. More accurate model calculates the ground state of the cell using a two state Hamiltonian and numerically solves the Schrödinger equation, which returns the Eigen energy for each of the wave states. The system evolves toward the ground state, therefore the lowest Eigen energy is chosen. This model has slower convergence times and is used to verify functionality of a design only into final stages.

III. BUILDING FLIP-FLOPS

A flip flop in essence is just an edge detector, but in being an edge detector it embodies in itself the essential nature of a counter, wherein it becomes possible to cascade several flip flops and build n-array counters. The inspiration for this design comes directly from the way flip flops (edge detectors) are built in traditional CMOS circuits.

There are two different ways flip flops arise in traditional circuitry. This circuit design can be obtained from techniques of asynchronous design fairly easily, though at first there seems no intuitive way of getting at this circuit. Dr. Kolin Paul says [05] that we cannot construct an analogue of this design using Quantum Cellular Automata as we have no analogue of cross coupled NAND gates.

The QCA circuit layout for the master slave arrangement is shown in figure 1. The layout clearly shows two latches cascaded one after the other. This design uses 133 QCA cell and spans over 8 clocking zones from input to output. The input-output delay of the circuit is therefore 2 clock cycles. Although the translation of the design seems a very mechanical task, it is in fact a very tricky and non-trivial one particularly with respect to deciding the clocking zones. The layout shown in figure 4 took several iterations to come to its current working form.

- Figure 1. Negative edge triggered QCA based D-flip flop design
- Figure 2. Proposed design of JK flip-flop

A. Proposed design on J-K Flip-Flop

- Figure 3. Simulation result of J K flip-flop
cycles. Although the translation of the design seems a very mechanical task, it is in fact a very tricky and non-trivial one particularly with respect to deciding the clocking zones.

B. Proposed Design for RS Logic
This is the simulation result of J K flip flop for the input-output delay of the circuit is therefore 2 clock cycles. Although the translation of the design seems a very mechanical task, it is in fact a very tricky and non-trivial one particularly with respect to deciding the clocking zones.

![Figure 4. QCA RSLogic [07]](image)

This is the simulation result of RS flip flop for the input-output delay of the circuit is shown in figure 5. It is in fact a very tricky and non-trivial one particularly with respect to deciding the clocking zones.

![Figure 5. Simulation result of RS Logic.](image)

Currently, K.Wallus and his team are developing a hierarchical design flow which will allow for design and simulation of system blocks and facilitate their reuse in large designs. They are also working on fault tolerance simulations which test the robustness of a design to outside influences and fabrication tolerances not included in the ideal models.

IV. CONCLUSION
In the case of current driven circuits, when have a feedback loop, the current gives the needed directionality. It ensures the fact that to start at the input and end at the output going through a series of voltage changes along the way. However, in this case, there is no current and no directionality. It is a system which waits to settle in a stable ground state. This means that the concept of feeding output back into the input is equivalent to actually feeding the input into the output since there is no question of direction when there is no driver (cell of a forcing and fixed polarization), and our feedback loop has no driver. Hence as soon as one gets a closed loop without the sense of a driving signal that drives the next state, it is a system which just settles to some ground state.

As discussed, some design features such as inherent data flow control and some design limitations such as limited wire length and consumed area have led to growing attentions in replacement of CMOS structures with QCA ones. In QCA implementation of equivalent CMOS circuits, it is essential to consider the inherent characteristics of QCA technology instead of ordinary replacement of basic gates with the majority gates. The capability of developing precise timing of data flow must be noted as one of those inherent features in QCA.

V. FUTURE WORK
The proposed circuit is promising in future nanosacle ultra low power information processing systems and may improve speeds in the nanoarchitecture circuit. However, it should be pointed that QCA technologies are still being develop and the design rules are likely to change. This research opens the questions of circuit optimization.

REFERENCES
[6] Sanjukta Bhania and Saket Srivastava Bayesian Modeling of Quantum-Dot Cellular-Automata Circuits Department of Electrical Engineering University of South Florida, Tampa, USA (bhania, ssrivast)@eng.usf.edu Accepted for Publication in NSTI Nanotechnology Conference, 2005